

DETERMINISTIC OUTPUT RESPONSE ANALYZER

ABSTRACT

Circuits, methods, and apparatus for output response analyzers that may be used during integrated circuit testing. Embodiments of the present invention compare current output test data with previous output test data. In this way, repetitive test patterns such as checkerboards may be employed while limiting circuit complexity. Embodiments may further provide for the combining of outputs of several built-in self-test circuits into as few as one signal that may be provided as a test output.

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